PRELIMINARY AMENDMENT

Please add claims 6-14 to this application:

6. (New) A semiconductor device comprising:

a substrate, and

a multilayer formed on the substrate, the multilayer comprising a semiconductor element and a dummy semiconductor element,

wherein the semiconductor element includes a first dielectric layer and an electrode on the first dielectric layer, and the first dielectric layer is composed of the material selected from a dielectric material having a dielectric constant of 100 or more and a ferroelectric material, and

wherein the dummy semiconductor element includes a second dielectric layer and a dummy electrode on the second dielecric layer,

and

wherein the dummy semiconductor element is located so that a space between the electrode and the dummy electrode is in a predetermined range, and

wherein the multilayer is produced by a method comprising:

forming a dielectric film for the first dielectric layer and the second dielectric layer;

forming an electrically conductive film on the dielectric film;

and

etching the electrically conductive film so as to form the electrode and the dummy electrode.

7. (New) A semiconductor device according to claim 6, wherein the predetermined range of the space is between 0.3μm and 14μm.

8. (New) A semiconductor device according to claim 6, wherein the method further comprises etching the dielectric film so as to form the first dielectric layer and the second dielectric layer.

9. (New) A semiconductor device according to claim 6, wherein the electrode is surrounded by the dummy electrode.

10. (New) A semiconductor device according to claim 6, wherein the semiconductor device is a transistor in which the electrode works as a gate of the transistor.

11. (New) A semiconductor device according to claim 6, wherein the semiconductor device is a capacitor element further comprising a bottom electrode between the first dielectric layer and the substrate, and the dummy semiconductor element is a dummy capacitor element further comprising a dummy bottom electrode between the second dielectric layer and the substrate, and

wherein the method further comprises forming a bottom electrically conductive film for the bottom electrode and the dummy bottom electrode between the dielectric film and the substrate.

12. (New) A semiconductor device according to claim 7, wherein the space is 9 μm or less.

13. (New) A semiconductor device according to claim 7, wherein the space is 5μm or less.

14. (New) A semiconductor device according to claim 11, wherein the method further comprises etching the bottom electrically conductive film so as to form the bottom electrode and the dummy bottom electrode.

Offer to Surrender

The assignee, through the undersigned attorney of record, hereby offers the surrender of the original US Patent No. 6,320,214.

Respectfully submitted,

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DPM/jh